<u>REMARKS</u>

Claims 1-34 are pending. In the Office Action dated January 30, 2006, the Examiner took the following action: (1) rejected claims 1-34 under 35 U.S.C. § 112, second paragraph, as failing to distinctly claim the subject matter; (2) rejected claims 1, 3, 7-10, 11, 13, 17-20 and 31-34 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,970,968 to Holman ("Holman") in view of U.S. Patent Application Publication No. 2004/0123180 to Soejima et al. ("Soejima"); (3) rejected claims 2, 12 and 34 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima as applied to claims 1, 11 and 31 above, and further in view of U.S. Patent No. 5,274,584 to Henderson et al. ("Henderson"); (4) rejected claims 4 and 14 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima as applied to claims 1 and 11 above and further in view of U.S. Patent No. 5,619,676 to Fukuda et al. ("Fukuda"); (5) rejected claims 5 and 15 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima as applied to claims 1 and 11 above and further in view of U.S. Patent Application Publication No. 2004/0123043 to Rotithor et al. ("Rotithor"); (6) rejected claims 6 and 16 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima as applied to claims 1 and 11 above and further in view of U.S. Patent No. 5,768,152 to Battaline et al. ("Battaline"); (7) rejected claims 21, 23 and 27-30 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima and applicant's admitted prior art; (8) rejected claim 22 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima and applicant's admitted prior art as applied to claim 21 above and further in view of Henderson; (9) rejected claim 24 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima and applicant's admitted prior art as applied to claim 21 above and further in view of Fukuda; (10) rejected claim 25 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima and applicant's admitted prior art as applied to claim 21 above and further in view of Rotithor; and (11) rejected claim 26 under 35 U.S.C. § 103(a) as being obvious over Holman in view of Soejima and applicant's admitted prior art as applied to claim 21 above and further in view of Battaline.

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the

scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The disclosed invention is directed to a memory module having a plurality of memory devices and a memory hub, configured to optimize the performance of a memory system over prior art memory modules with a memory hub architecture. The memory module contains memory devices typically used in computer systems, such as dynamic random access memory ("DRAM") devices for storing data that are accessed by a processor. According to an embodiment of the invention, several of the memory modules are coupled to a system controller, which serves as a communication path to the processor for a variety of components, including the system memory. The memory modules are coupled to the system controller through a high-speed link, which may be an optical or electrical communication path or some other type of communication path. Each of the memory modules includes a memory hub for controlling access to the memory devices and to efficiently route memory requests and responses between the system controller and the memory devices. The memory hub includes a number of features, which in combination work to improve the overall performance of the memory system. In particular, the memory hub includes a performance monitor that is operable to track at least one performance metric.

With reference to Figure 2, the metric tracked by the disclosed performance monitor 290 may be from a group of metrics that include page hit rate, number or percentage of prefetch hits, cache requests, rate or percentage of memory bus utilization, local hub request rate or number, and remote hub request rate or number. The performance monitor 290 also monitors the transmission of memory requests and data through the memory hub 200 to determine how busy the hub is and how efficiently the memory requests and data are being transmitted without excessive delay.

The Office Action cites the patent to Holman, which describes a memory module controller serving as an interface between a system memory controller and a plurality of memory devices on a memory module. The memory module controller described by the Holman patent is of the type disclosed in the present application as the prior art memory hub architecture. Such memory hub architecture may also be efficient at routing memory requests and responses between the system controller and the memory devices, and typically include configurations

having increased bandwidths for speedier data transfer. However, as the present application describes, conventional memory hub architectures generally have other limitations that continue to slow the operating speed of the entire system. It is difficult to diagnose what causes the latency problems in memory systems, even in systems with the conventional memory hubs. Although, the Holman patent describes a method for improving the operating speed of memory systems by using memory hubs, none of the embodiments of the Holman patent describe conducting a performance test on the memory devices or the memory hub to optimize the performance of the memory system. In contrast, applicant's disclosed memory hub includes a performance monitor to diagnose the performance of various components of the memory system, thereby having improved operating speeds over systems with conventional hub architecture. The Holman patent also does not provide any reason to modify its teaching to include a performance monitor coupled to the memory device interface for tracking one or more performance metrics.

The Office Action also cites the patent to Soejima, which purportedly teaches modifying the disclosure of the Holman reference, to incorporate a performance measurement unit in the memory module controller for measuring various performance metrics as the system memory devices are accessed. The Soejima patent is instead directed to maintaining the overall performance of a "cluster system", a system which combines two or more computers operating as a single system. For example, the failover cluster system described by the Soejima patent has an active server and a standby server that share volumes of data from a network of computers, and maintains copies of those volumes. The computer data are stored in these storage apparatuses, and the destination to the volumes of data within these units are defined by a parity group coding system. The storage apparatuses also include a performance information management unit that manages the performance of the parity groups and access to the volumes of data, and then stores the performance information. The performance information management unit is not concerned with monitoring the particular efficiency of a memory hub as it transmits memory requests and memory data to DRAM or other memory devices within a memory system. The performance information management unit of the Soejima patent analyzes different types of data, namely data for accessing volumes of stored data shared by multiple computers, and not data relating to the performance of accessing the system memory within a single computer. Therefore, the Soejima reference does not teach or suggest a performance monitor for tracking

one or more metrics associated with memory device access, or for determining the efficiency of how data is transmitted by the memory hubs of memory modules within a computer.

Applicant understands that the motivation to modify a reference does not need to be expressly articulated by the cited references, although if there is motivation to combine or modify a reference, such motivation is usually expressly found in the references. However, the Examiner still must articulate a credible motivation to modify the cited references, either from the express or implied teachings of the cited reference or from knowledge commonly known to those of ordinary skill in the art. A reason has not been articulated why one of ordinary skill in the art would modify a conventional memory hub of the Holman reference to incorporate a performance information management unit of the Soejima reference for monitoring the performance of a memory system within a single computer system. The Soejima reference only describes a performance information management unit configured to manage the performance of accessing stored volumes of computer data stored in an external storage apparatus shared by multiple computers. Combining the Holman and Soejima references may suggest improving the performance of accessing stored volumes of data in a cluster of several computers with memory systems having the Holman memory hub. However, nothing suggests modify the internal components of each computer, such as memory devices, to perform a diagnosis for improving the overall performance of each individual computer.

In summary, there is simply no teaching, either expressed or implied, in the combination of teachings of the Holman and Soejima references to suggest including a performance monitor in the memory hub of a memory module to track the performance of the memory system while accessing a plurality of memory devices.

Turning now to the claims, amended claim 1 is directed to a memory module having a plurality of memory devices and a memory hub. The memory hub further includes a link interface for receiving memory requests for access to memory cells in at least one of the memory devices. The memory hub also includes a memory device interface operable to transmit memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests. The memory hub also includes a performance monitor coupled to the memory device interface, operable to track at least one performance metric. As stated by the Office Action, the Holman

patent does not disclose a memory module that includes a memory hub having a performance monitor to track one or more performance metrics. Furthermore, there is no motivation or suggestion to combine the Holman reference and the Soejima reference to achieve the present invention of claim 1, as explained above.

Amended claim 11 is directed to a memory hub that includes a link interface and a memory device interface to transmit memory requests to the memory devices for accessing memory cells. As in claim 1, the memory hub of claim 11 also includes a performance monitor coupled to the memory device interface, and operable to track at least one performance metric. In particular, the combination of the Holman and Soejima references does not teach or suggest a memory hub that includes a performance monitor to monitor the performance of the memory system or the memory hub, as already described.

Amended claim 21 is directed to a computer system that includes a plurality of memory modules having a plurality of memory devices and a memory hub. The memory hub of the computer system in claim 21, like the memory hub of claim 11, includes a link interface for receiving memory requests, a memory device interface to transmit memory requests to the memory devices and to receive read data, and a performance monitor coupled to the memory device interface to track at least one performance metric. The patent to Soejima is directed to a performance information maintenance unit contained in an external storage apparatus shared by multiple computers. The combined teachings of the Holman and Soejima references do not teach a memory hub with a performance monitor, as previously described.

Amended claim 31 is directed to a method of reading data from a memory module. The method includes transmitting memory requests to the memory device responsive to received memory requests with at least some of the memory requests being memory requests to read data, and tracking at least one performance metric within the memory module. The combination of the Holman and Soejima references does not teach or suggest a method of transmitting memory requests to the memory device and tracking at least one performance metric to monitor the performance of the memory system, as previously described.

Claims depending from claims 1, 11, 21 and 31 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. For example, as described by claims 8, 18, 28 and 32, tracking the at

least one performance metric may be selected from the group of metrics that include page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests, rate or percentage of memory bus utilization, local hub request rate or number, and remote hub request rate or number. None of the cited references discloses or fairly suggest memory hub architecture having a performance monitor that uses any one of these metrics when monitoring the memory system or memory hub itself.

Additionally, claims 1, 10, 11, 19, 21, 30 and 31 are amended to obviate the Section 112 rejection. The amendments do not affect the scope of claims 1, 10, 11, 19, 21, 30 and 31, but merely improves its form.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP

Edward W. Bulchis
Registration No. 26,847
Telephone No. (206) 903-8785

EWB:dms

Enclosures:
    Postcard
    Fee Transmittal Sheet (+sheet)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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